	Application No.	Applicant(s)
Notice of Allowability	09/684,328	OHARA ET AL.
	Examiner	Art Unit
	Joni Hsu	2671
	30	2071
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to papers received December 13, 2005.		
2. The allowed claim(s) is/are <u>1-25</u> .		
 3. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some* c) None of the: 1. Certified copies of the priority documents have been received. 		
2. Certified copies of the priority documents have been received in Application No		
3. Copies of the certified copies of the priority documents have been received in this national stage application from the		
International Bureau (PCT Rule 17.2(a)).		
* Certified copies not received:		
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		
4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.		
5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.		
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached		
1) hereto or 2) to Paper No./Mail Date		
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date		
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).		
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.		
Attachment(s) 1. ☑ Notice of References Cited (PTO-892)	5. ☐ Notice of Informal P	atent Application (PTO-152)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)	6. Interview Summary	(PTO-413),
3. Information Disclosure Statements (PTO-1449 or PTO/SB/0	Paper No./Mail Da 08), 7. ⊠ Examiner's Amendr	
Paper No./Mail Date 4. Examiner's Comment Regarding Requirement for Deposit	8. 🛛 Examiner's Stateme	ent of Reasons for Allowance
of Biological Material	9.	

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DETAILED ACTION

Response to Amendment

1. Applicant's arguments, see pages 12-22, filed December 13, 2005, with respect to Claims 1-25 have been fully considered and are persuasive. The 35 U.S.C. 103(a) rejections of Claims 1-25 has been withdrawn.

EXAMINER'S AMENDMENT

- 2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.
- 3. The application has been amended as follows:

In Claims 1, 2, 7, and 11, the phrase "generating transfer packets each including at least one of *one or more* said plurality of drawing commands" is changed to "generating transfer packets each including at least one of said plurality of drawing commands."

Allowable Subject Matter

4. Claim 1-25 are allowed.

The following is an examiner's statement of reasons for allowance:

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5. The prior art taken singly or in combination do not teach or suggest translating the merged drawing commands into a single drawing command and generating transfer packets each including at least one of the plurality of drawing commands whose amount is within a certain predetermined range and one or more merged drawing commands, as recited in Claims 1, 2, 7, and 11. Claims 3-6, 8-10, and 12-25 depend from these claims, and therefore also contain allowable subject matter.

The closest prior art (Yutaka US 5,664,163) teaches a data transferring apparatus for 6. transferring transfer packets each including one or more transfer data as objectives of transfer from a first apparatus (42, 43, 45, Figure 1) to a second apparatus (61), each transfer data including commands indicating processes against a preliminarily assigned area, the first apparatus including a scheduler for merging a plurality of drawing commands (43; Col. 6, lines 65-67; Col. 7, lines 1-13). Yutaka describes that in the prior art, sometimes the drawing instructions are shorter than the packet are frequency used, and there occur many inefficient transfer operations (Col. 2, lines 17-34), meaning that there is a large volume of transfer data. Therefore, Yutaka translating the merged drawing commands into a drawing instruction sequence, thereby reducing a volume of the transfer data (Col. 2, lines 17-24; Col. 7, lines 1-13); and a communication controller (42) for generating transfer packets each including at least one of one or more plurality of drawing commands whose amount is within a certain predetermined range (Col. 2, line 15), the communication controller transferring the generated transfer packets to the second apparatus (45; Col. 3, lines 12-14). However, Yutaka does not teach translating the merged drawing commands into a single drawing command.

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Another prior art (Mills US006563505B1) teaches a graphics controller circuit that translates the merged commands into a single command, thereby reducing a volume of the transfer data (Col. 2, lines 45-53). Mills describes that although the present invention is explained with reference to a move display block operation, it will be appreciated that it is within the scope and spirit of the present invention to perform other types of operations (Col. 4, lines 33-37). However, Mills does not teach generating transfer packets each including at least one of the plurality of drawing commands whose amount is within a certain predetermined range and one or more merged drawing commands.

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- 8. Another prior art (Peaslee US 5,265,203) teaches a scheduler, which Peaslee calls a cogenerator (10, Figure 1), that has a multiprocess scheduler (12, Figure 2; Col. 5, lines 5-12) that prevents the subsystems from using the same output at the same time (Col. 5, lines 50-59). However, the scheduler in Peaslee enables or disables subsystems, instead of merging data, in accordance with their input/output dependencies.
- Another prior art (Baber US006279041B1) teaches that the means for merging comprises a scheduler for judging whether an offset can be performed by merging an increment of data volume caused by a change of commands (Col. 14, lines 49-50; Col. 15, lines 26-35; Col. 18, lines 1-3). However, Applicant has submitted an affidavit to overcome this reference.

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10. Another prior art (Nitta US006392619B1) teaches the data transfer of images for which the same data is continuously transferred (Col. 9, lines 7-10), meaning that the first apparatus and the second apparatus generate identical images. Nitta describes a different timing due to a data transfer delay from the first apparatus to the second apparatus (Col. 10, lines 59-67). However, Nitta does not teach merging graphics commands.

- 11. Another prior art (Zhao US006405267B1) teaches generating the drawing commands to be transferred from the first apparatus (CPU) to the second apparatus (graphics device) (Col. 1, lines 21-30) by ordering the drawing commands (Col. 2, lines 43-59) by putting the drawing commands into slots in the storage buffers, the slot selected based on portions of the address information associated with the data item. The data in the storage buffers is then provided to a command interpreter for further processing by the graphics device (Col. 3, lines 21-35). Therefore, Zhao discloses combining or merging an effect of the plurality of drawing commands which affect a same area. The storage buffers receive these drawing commands from the FIFO, which outputs the drawing commands at graphics device clock rate (Col. 3, lines 21-35). This means that the drawing commands that are combined or merged which affect a same area are effective for a predetermined short period of time on a frame buffer, the predetermined short period of time being in accordance with the graphics device clock rate. However, Zhao does not reduce the data volume, according to the claimed invention.
- 12. Another prior art (Tidwell US006437789B1) describes that if a slot 12 of the write cache 24 has been changed, and needs to be written to the DRAM, a "dirty" flag is set for that slot until

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the data is written back to the DRAM (Col. 7, lines 61-64). The cache memory is part of the frame buffer (Col. 4, lines 2-4). The graphics commands cause the graphics memory to store pixel data received from the write cache memory (Col. 11, lines 33-39). Therefore, only the updated areas on a frame memory are transferred by analyzing graphics commands in a form of drawing commands from the first apparatus (24) to the second apparatus (DRAM). However, Tidwell needs to execute all graphics commands before merging their outputs.

Another prior art (Epard US005241625A) teaches that the first apparatus (50, Figure 5A) 13. includes a first drawing engine (55) and the second apparatus (60) includes a second drawing engine (61) (Col. 48, lines 26-57). Epard describes that the first apparatus (50, Figure 5A) and the second apparatus (60) display the same information (Col. 3, lines 5-43). Therefore, Epard describes that the first apparatus and the second apparatus include redundant drawing engines (55, 61) because both drawing engines process the same information.

However, Epard does not teach that the first apparatus merges graphics commands to reduce the amount of the data volume that the first apparatus transmits to the second apparatus.

Any comments considered necessary by applicant must be submitted no later than the 14. payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Prior Art of Record

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The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- 1. Yutaka (US 5,664,163) teaches an image generating method of transferring drawing instructions and control instructions generated by a CPU to a drawing device section, and generating an image in the drawing device section by sequentially performing drawing operations in accordance with the drawing instructions and the control instructions (Col. 2, lines 45-52).
- 2. Mills (US006563505B1) teaches a graphics controller circuit including a host interface which may receive a command from the host, and generate a plurality of instructions from the command (Col. 2, lines 30-32).
- 3. Peaslee (US 5,265,203) teaches an integrated hardware multiprocess scheduler that control of a plurality of concurrently operating graphics subfunctions required from the generation of display signals for a graphics rendering processor (Col. 2, lines 18-22).
- 4. Baber (US006279041B1) teaches improved performance for data communications in a low-speed communication environment such as wireless communications (Col. 2, lines 34-37).
- 5. Nitta (US006392619B1) teaches a data transfer device and a liquid crystal display device which can reduce the power consumption in a data bus (Col. 1, lines 49-52).

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- 6. Vegesna (US 5,640,588) teaches a scheduler (2, Figure 18) for merging a plurality of transfer data in accordance with the mutual dependency of the instructions among themselves (Col. 3, lines 12-37; Col. 23, lines 6-20). Vegesna also teaches that when there are data dependencies between instructions, they cannot be issued simultaneously (Col. 33, lines 38-40), and Vegesna suggests the advantage of achieving multiple launches and executions of the instructions by merging the data in accordance with the mutual dependency of the instructions among themselves (Col. 3, lines 12-37). Vegesna discloses both the apparatus and method (Col. 1, line 12). The details of the method for merging a plurality of transfer data in accordance with the mutual dependency of the instructions among themselves are described in Col. 26, lines 4-62.
- Zhao (US006405267B1) teaches systems and methods of increasing effective bus bandwidth through utilization of commanding encoding in a weakly ordered bus interface (Col. 2, lines 43-45).
- 8. Tidwell (US006437789B1) teaches providing a method and apparatus for balancing cache throughput and latency in accordance with the type of accesses being made of cache (Col. 2, lines 34-36).
- 9. Epard (US005241625A) teaches a system for sharing computer screen information among homogeneous and heterogeneous computers (Col. 3, lines 30-36).

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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